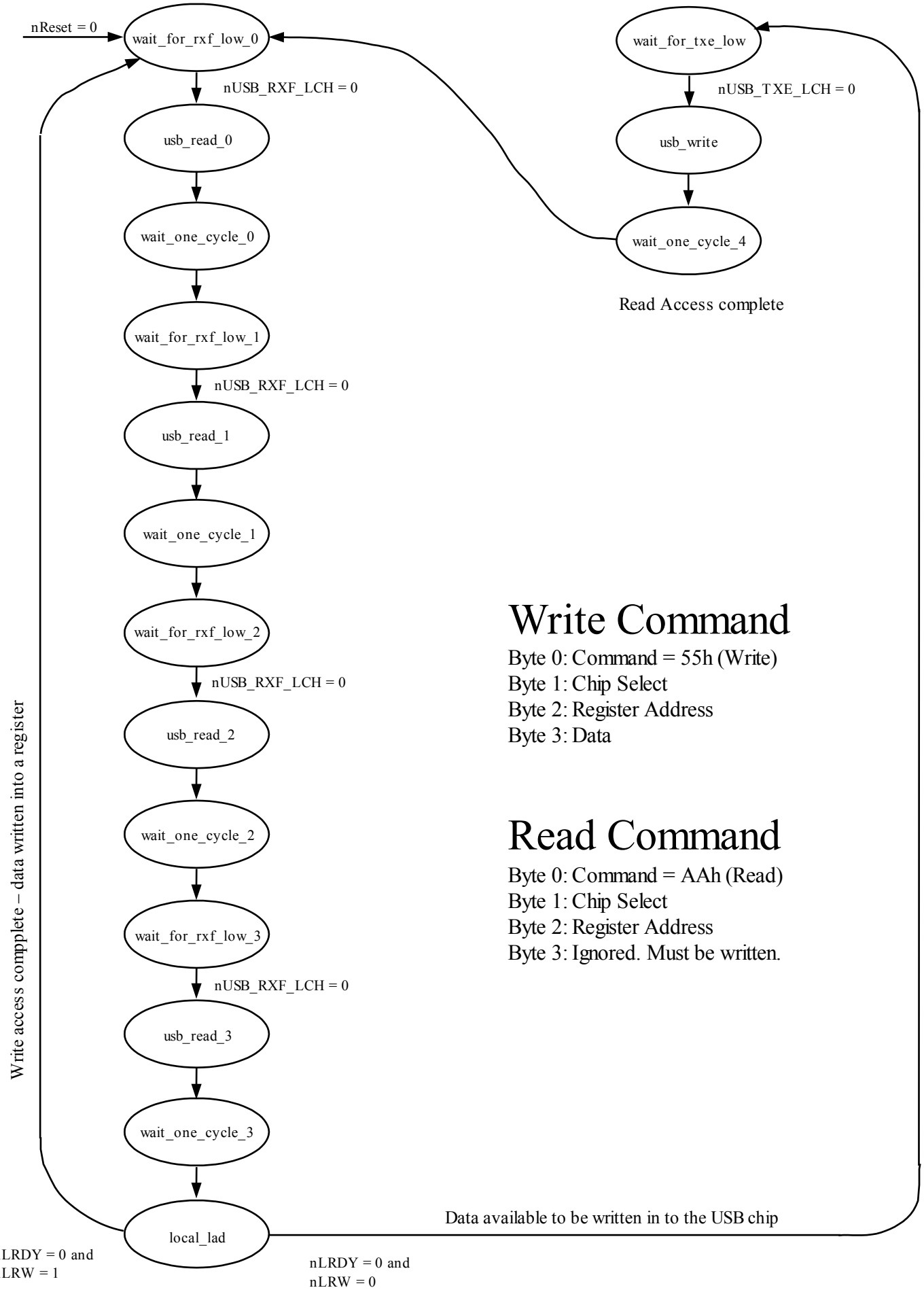
Sample2.vhd State Machine State Diagram



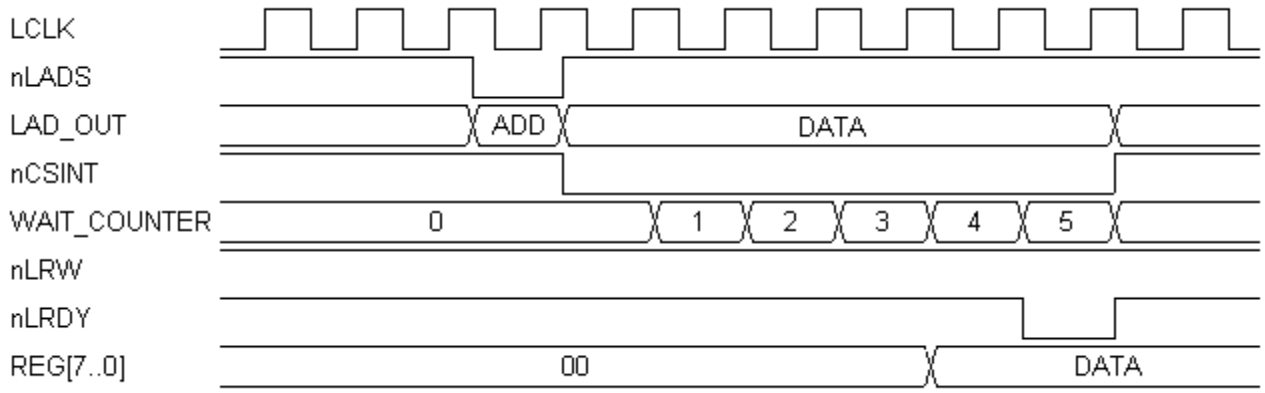
Write Command

Byte 0: Command = 55h (Write)
Byte 1: Chip Select
Byte 2: Register Address
Byte 3: Data

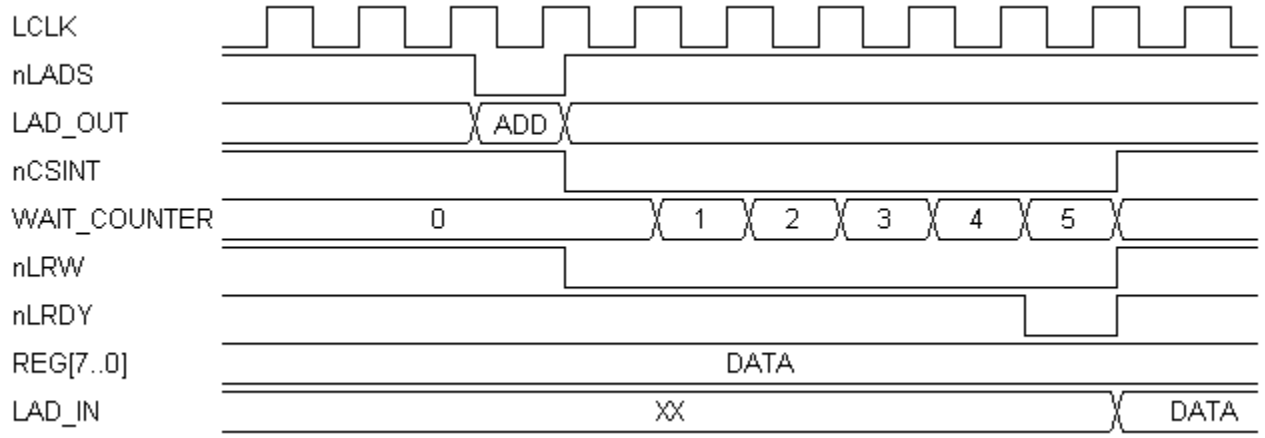
Read Command

Byte 0: Command = AAh (Read)
Byte 1: Chip Select
Byte 2: Register Address
Byte 3: Ignored. Must be written.

Sample2.vhd Register Access



Register Access - Write



Register Access - Read

Sample2.vhd Memory Map

FPGA Revision Number

CS = 00h, Address: 00h, Type: R/O

LED Register

CS = 00h, Address: 01h, Type: R/W